WHAT IS CLAIMED IS:

1. A data writing method of a nonvolatile semiconductor memory device to reprogrammable nonvolatile semiconductor memory for storing N ($N \geq 3$) level of multilevel data by repeating a verification cycle of a write operation, a verify-read operation, and a compare operation until a write threshold level to a nonvolatile semiconductor memory cell exceeds a write level corresponding to an expected level, comprising the steps of:

invalidating a verification result of a memory cell where a Nth threshold level which is a highest level is to be written as an expected level by mandatorily setting the verification result to "FAIL" until completion of writing to a memory cell where a (N-1)th and lower threshold level is to be written; and

validating a verification result of the memory cell where the Nth level is to be written after reaching the (N-1)th write level.

2. A data writing method of the nonvolatile semiconductor memory device according to Claim 1, wherein a reference current supplied to a sense amplifier corresponding to the Nth threshold level which is a highest level as an expected level is set at at least a level allowing no indeterminate sensing of the sense amplifier, and a word line voltage supplied for the verify-reading in verification of the Nth level data is switched to a second word

line voltage higher than a first word line voltage supplied in verification of the (N-1)th and lower level data.

3. A data writing method of the nonvolatile semiconductor memory device according to Claim 2, wherein a write threshold level to the memory cell where the Nth level is to be written is set at at least the first word line voltage.

4. A data writing method of the nonvolatile semiconductor memory device according to Claim 2, wherein a reference current for verification supplied to the sense amplifier corresponding to the Nth level is set equal to a reference current supplied in data reading from the nonvolatile semiconductor memory storing multilevel data.

5. A data writing method of the nonvolatile semiconductor memory device according to Claim 2, wherein a verification result of the memory cell where (N-1)th and lower level data is to be written is mandatorily set to "PASS" while a verification result of the Nth data is valid to stop a writing operation to the memory cell where (N-1)th and lower level data is written.

6. A reprogrammable nonvolatile semiconductor memory device for storing multilevel data, comprising

a power unit for supplying a predetermined word voltage to

a word line to which a nonvolatile semiconductor memory cell is connected, capable of switching the word voltage between a first predetermined word line voltage and a second predetermined word line voltage higher than the first word line voltage;

a data writing control circuit for controlling data writing to the nonvolatile semiconductor memory cell, comprising:

an I/O buffer for inputting N ($N \geq 3$) level write data specified by a user to the nonvolatile semiconductor memory cell;

a data register for holding the write data from the I/O buffer and outputting the write data as expected level data;

a write circuit for performing data writing to the nonvolatile semiconductor memory cell;

(N-1) number of sense amplifiers for reading out a write level state of the nonvolatile semiconductor memory cell;

a decoder for decoding a write level of the memory cell read out by the sense amplifiers;

a compare circuit for comparing data decoded by the decoder with the expected level data retained in the data register and outputting a verification result;

a selection circuit for selecting between an output from the compare circuit and an output for mandatorily setting a verification result to "FAIL", and outputting a selected one as a verification result; and

a selection signal generating circuit for outputting to the selection circuit a control signal for mandatorily setting

a verification result of a memory cell where a Nth threshold level which is a highest level is to be written as an expected level to "FAIL" until completion of writing to a memory cell where a (N-1)th and lower threshold level is to be written as an expected level and validating a verification result of the memory cell where the Nth level is to be written after reaching the (N-1)th write level, and outputting to the power unit a control signal for switching a word line voltage for verification between the first word line voltage in writing the (N-1)th and lower level and the second word line voltage in writing the Nth level; and

an array of nonvolatile semiconductor memory cells for storing one of N ($N \geq 3$) level data by repeating a verification cycle of a write operation, a verify-read operation, and a compare operation until a write threshold level to a nonvolatile semiconductor memory cell exceeds a write level corresponding to an expected level.

7. A nonvolatile semiconductor memory device for storing multilevel data according to Claim 6, wherein a plurality of the data writing control circuits are provided for simultaneous writing of data to a plurality of the nonvolatile semiconductor memory cells, and the power unit is controlled by an output from an AND gate to which a control signal output from each selection signal generating circuit of the plurality of the data writing control circuits is input.

8. A nonvolatile semiconductor memory device for storing multilevel data according to Claim 6, wherein a reference current supplied to a sense amplifier corresponding to the Nth threshold level which is a highest level as an expected level is set at at least a level allowing no indeterminate sensing of the sense amplifier.

9. A nonvolatile semiconductor memory device for storing multilevel data according to Claim 8, wherein a reference current supplied to the sense amplifier corresponding to the Nth level is set equal to a reference current supplied in data reading from the nonvolatile semiconductor memory storing multilevel data.

10. A nonvolatile semiconductor memory device for storing multilevel data according to Claim 6, wherein the data register has a function that rewrites expected level data retained therein into data for mandatorily setting a verification result to "PASS" upon receiving a "PASS" signal indicating completion of writing to the memory cell from the selection circuit.

11. A nonvolatile semiconductor memory device for storing multilevel data according to Claim 6, comprising a unit for mandatorily setting a verification result of the memory cell where (N-1)th and lower level data is written to "PASS" while a

verification result of the Nth data is valid.

12. A data writing method of a nonvolatile semiconductor memory device to reprogrammable nonvolatile semiconductor memory for storing N ($N \geq 3$) level of multilevel data by repeating a verification cycle of a write operation, a verify-read operation, and a compare operation until a write threshold level to a nonvolatile semiconductor memory cell exceeds a write level corresponding to an expected level, comprising the steps of:

setting a word line voltage supplied for the verify-reading in verification of the (N-1)th and lower level data to a first word line voltage; and

setting a word line voltage supplied for the verify-reading in verification of the Nth level data to a second word line voltage which is higher than the first word line voltage.

13. A data writing method of the nonvolatile semiconductor memory device according to Claim 12, further comprising the steps of:

invalidating a verification result of a memory cell where a Nth threshold level which is a highest level is to be written as an expected level by mandatorily setting the verification result to "FAIL" until completion of writing to a memory cell where a (N-1)th and lower threshold level is to be written; and

validating a verification result of the memory cell where

the Nth level is to be written after reaching the (N-1)th write level.

14. A data writing method of the nonvolatile semiconductor memory device according to Claim 12, wherein a reference current supplied to a sense amplifier corresponding to the Nth threshold level which is a highest level as an expected level is set at at least a level allowing no indeterminate sensing of the sense amplifier.

15. A data writing method of the nonvolatile semiconductor memory device according to Claim 12, wherein a write threshold level to the memory cell where the Nth level is to be written is set at at least the first word line voltage.

16. A data writing method of the nonvolatile semiconductor memory device according to Claim 12, wherein a reference current for verification supplied to the sense amplifier corresponding to the Nth level is set equal to a reference current supplied in data reading from the nonvolatile semiconductor memory storing multilevel data.

17. A data writing method of the nonvolatile semiconductor memory device according to Claim 12, wherein a verification result of the memory cell where (N-1)th and lower level data is to be

written is mandatorily set to "PASS" while a verification result of the Nth data is valid to stop a writing operation to the memory cell where (N-1)th and lower level data is written.

18. A reprogrammable nonvolatile semiconductor memory device for storing multilevel data, comprising

a power unit for supplying a predetermined word voltage to a word line to which a nonvolatile semiconductor memory cell is connected, capable of switching the word voltage between a first predetermined word line voltage and a second predetermined word line voltage higher than the first word line voltage;

a data writing control circuit for controlling data writing to the nonvolatile semiconductor memory cell, comprising:

an I/O buffer for inputting N ($N \geq 3$) level write data specified by a user to the nonvolatile semiconductor memory cell;

a data register for holding the write data from the I/O buffer and outputting the write data as expected level data;

a write circuit for performing data writing to the nonvolatile semiconductor memory cell;

(N-1) number of sense amplifiers for reading out a write level state of the nonvolatile semiconductor memory cell;

a decoder for decoding a write level of the memory cell read out by the sense amplifiers;

a compare circuit for comparing data decoded by the decoder with the expected level data retained in the data register

and outputting a verification result; and

a selection signal generating circuit for outputting to the power unit a control signal for switching a word line voltage for verification between the first word line voltage in writing the (N-1)th and lower level and the second word line voltage in writing the Nth level; and

an array of nonvolatile semiconductor memory cells for storing one of N ($N \geq 3$) level data by repeating a verification cycle of a write operation, a verify-read operation, and a compare operation until a write threshold level to a nonvolatile semiconductor memory cell exceeds a write level corresponding to an expected level.